Ka-BAND MONOLITHIC BROADBAND LNA MODULES

N. CAMILLERI, and P. CHYE

Avantek Incorporated
104 Woodmere Road
Folsom, CA 95630

ABSTRACT

A set of broadband monolithic GaAs MESFET low noise amplifiers (LNAs) have been developed. These Ka-band amplifiers make use of state of the art sub .25 um MESFET devices. Typical performance for a single stage LNA using a 75um device is about 5 dB of gain with an average noise figure of 4.5 dB across the 26.5 to 40 GHz band. A two stage monolithic chip has 10 dB of gain with an average noise figure of 6 dB across the Ka-band.

INTRODUCTION

Recent advances in GaAs low noise MESFET technology have made it possible to build broadband LNAs at Ka-band. This paper describes some of the first monolithic LNAs with reactive matching that cover the full Ka-band. These chips make use of a sub .25 um MESFET process to achieve less than 4.5 dB of noise figure with more than 5 dB gain per stage. Data on a two stage monolithic chip is also given. Although the noise figure of these MESFETs is slightly higher than that of a HEMT they are still good candidates for monolithic integration since the yields are high and the performance is predictable. Monolithic amplifiers reported in the literature (1) recently using HEMT devices does not show any superior performance to these MESFET chips.

DEVICE AND FABRICATION

The devices used in this monolithic design were made using either VPE or MBE materials. Both materials produce similar device performance and the VPE material is preferred for production runs since it is a less expensive material. The gates were defined using electron-beam lithography resulting in gate lengths ranging from .15 to .2um. The gate cross sectional area was also increased by making it in the shape of a mushroom in order to reduce gate resistance. Figure 1 shows an SEM micrograph of the typical cross section of the mushroom gates. The device used in this design consisted of a 75 um device with a T layout which consists of a single feed perpendicular to two gate fingers of 37.5 um length. Figure 2 shows an SEM micrograph of a test device used to measure S-parameters of the devices. From measured S-parameters the F_t is higher than 60 GHz and the F_{max} is higher than 120 GHz for these MESFETs.

Typical performance of these devices when tuned narrowband in a hybrid circuit at 35 GHz is 6dB gain with 3.5dB noise figure. Other MESFET structures with lower noise figures are available (2.2 dB at 35 GHz) but these monolithic runs made use of an inferior low noise device since they were contained on a mask together with power MESFETs and a compromise between power density and noise figure was made.

CH2725-0/89/0000-0533$01.00 © 1989 IEEE

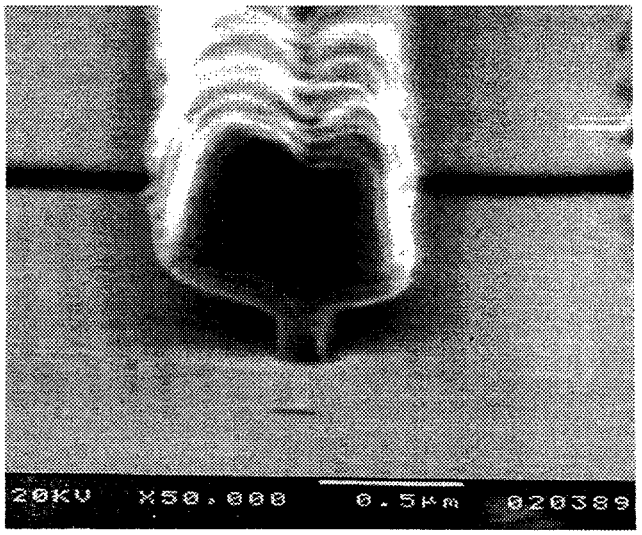


Figure 1. Cross sectional SEM micrograph of the sub .25 um mushroom gate.

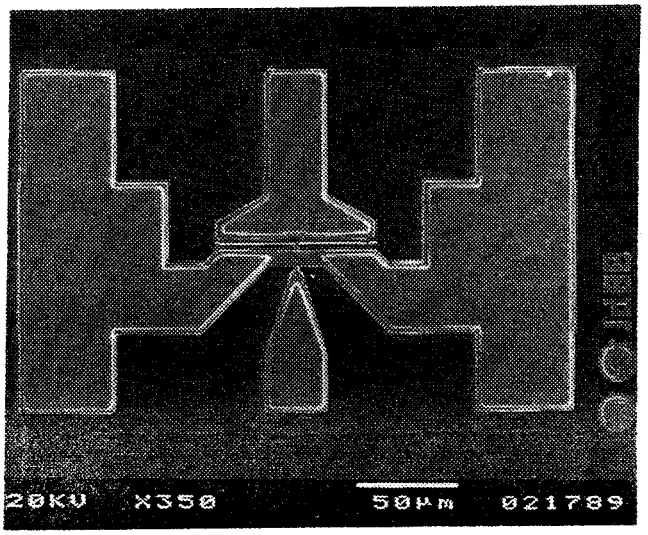


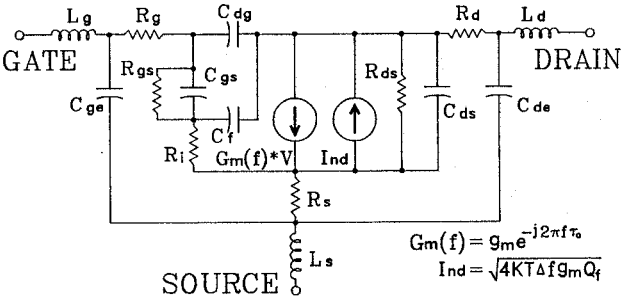
Figure 2. SEM micrograph of the 75 um MESFET.

The monolithic design made use of via-holes for source grounding, air bridges for interconnect, and MIM capacitors using silicon nitride for RF grounding and dc blocking. In order to increase the yield and avoid reliability problems the MIM capacitors were not placed on top of via holes in this design.

The Ka-band monolithic design relied on accurate device modeling in order to have a first cut success. The model was derived from S-parameter data taken up to 26.5 GHz. With the aid of on wafer probing accurate S-parameter data was available which made it easy to construct an accurate small signal model. The element values of the 75um device used in this monolithic design is shown in Figure 3.

SINGLE STAGE MONOLITHIC AMPLIFIER

The amplifier design made use of small signal analysis to establish a broadband design. Both input and output matching circuits consisted of a similar two pole matching topology. The topology consists of a series transmission line from the FET followed by an inductive transmission line to ground via an MIM capacitor which is also used for biasing. These two elements are then followed by another



g_m (mS)	30
Q_f	2.2
τ_o (ps)	0.5
R_{gs} (Ω)	20000
R_I (Ω)	1.2
R_{ds} (Ω)	475
C_{gs} (pF)	.076
C_{dg} (pF)	.01
C_f (pF)	.034
C_{ds} (pF)	.005
R_g (Ω)	3.6
R_d (Ω)	3.0
R_s (Ω)	1.6
L_g (nH)	.01
L_d (nH)	.01
L_s (nH)	.025
C_{ge} (pF)	.01
C_{de} (pF)	.002

Figure 3. Small signal model for a 75x.2 um low noise MESFET.

series transmission line, and a shunt capacitive stub. This two pole matching technique can achieve the desired bandwidth to cover the whole Ka-band. The equivalent circuit for this design is shown in Figure 4. A CAD layout implementing the equivalent circuit shown in Figure 4 for the monolithic amplifier is shown in Figure 5. In this layout one can observe the redundancy of transmission lines and air-bridges put in place to facilitate tuning on the MMIC if required. Eventually no tuning was required to meet the expected goals from the MMIC. This success is attributed to the accurate device modeling and the consistency of the sub .25um MESFETs. The gain and noise figure of the amplifier is shown in Figure 6. This monolithic chip has demonstrated gain better than 5 dB with less than 2dB ripple and worst case noise figure of 6dB across the 26.5 to 40 GHz band. The noise figure is less than 4.5 dB across the 30 to 40 GHz band. These results show that the MESFET is competitive with recent reported data (1) for similar designs fabricated using HEMT material.

TWO STAGE MONOLITHIC AMPLIFIER

A two stage monolithic design has been implemented so that more gain per monolithic chip is obtained. The overall size of this chip will also be smaller than cascading two single stage chips since matching to 50 ohms between stages is not necessary thus achieving more gain per unit area of GaAs used. The matching topology for the input of the first stage and the output of the second stage are identical to that of the single stage design. The interstage matching also consisted of a two pole matching topology. The equivalent circuit and element values for this two stage design is shown in Figure 7. Starting at the output of the first stage the interstage topology consists of a series transmission line followed by an inductive transmission line to ground via an MIM capacitor which is used for biasing the drain of the first stage. At this point a dc blocking capacitor (3 pF in value) is added in series. Due to the high value of capacitance at 26 GHz this capacitor does not contribute much to the RF circuit other than the stray capacitance to ground introduced due to its physical

All dimensions in um.

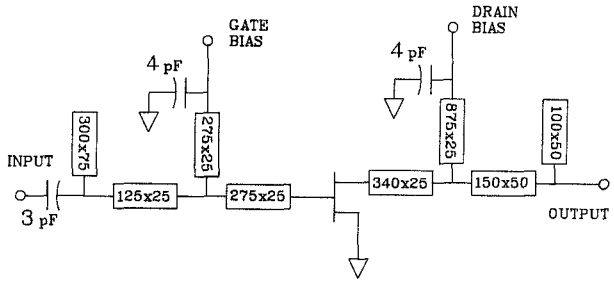


Figure 4. Equivalent circuit and element values for a single stage monolithic Ka-band MESFET LNA.

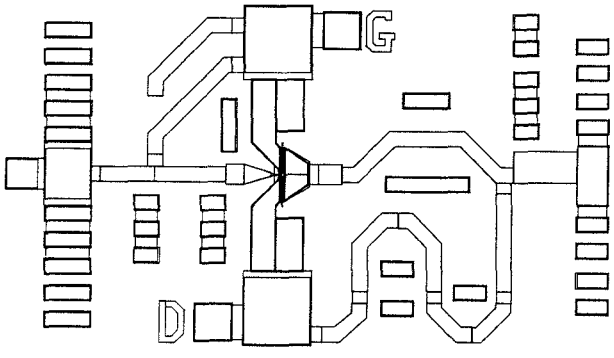


Figure 5. CAD layout for the single stage broadband monolithic Ka-band LNA.

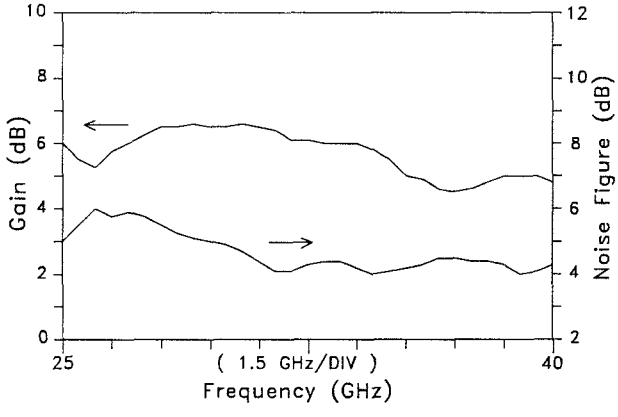


Figure 6. Measured performance for a single stage monolithic amplifier using a 75 um MESFET.

geometry. The circuit is then followed by an other series transmission line, an inductive transmission line to ground (also used to bias the gate of the second stage), and another series transmission line.

A CAD layout implementing the equivalent circuit shown in Figure 7 for the monolithic two stage amplifier is shown in Figure 8. Similar to the single stage design the layout has redundancy of transmission lines and air-bridges put in place to facilitate tuning on the MMIC if required. Eventually no tuning was required to meet the expected goals from the two stage MMIC. The gain and noise figure of the amplifier is shown in Figure 9. This monolithic chip has demonstrated gain better than 10 dB and worst case noise figure of 7.5 dB across the 26.5 to 40 GHz band. The noise figure is lower than 6 dB across the 28 to 40 GHz band. These results are consistent with the single stage design and the higher noise measurement is due to the second stage contribution.

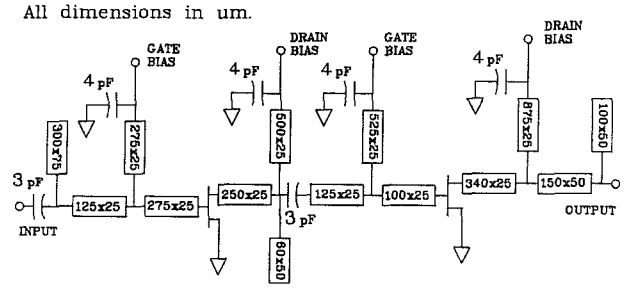


Figure 7. Equivalent circuit and element values for a two stage monolithic 26.5 to 40 GHz MESFET LNA.

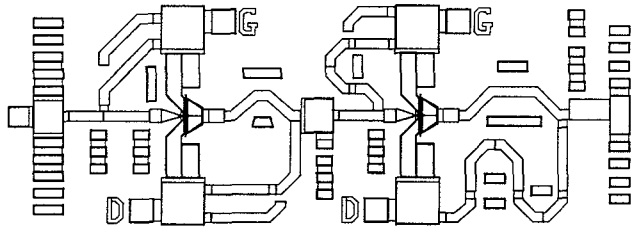


Figure 8. CAD layout for the two stage broadband monolithic Ka-band LNA.

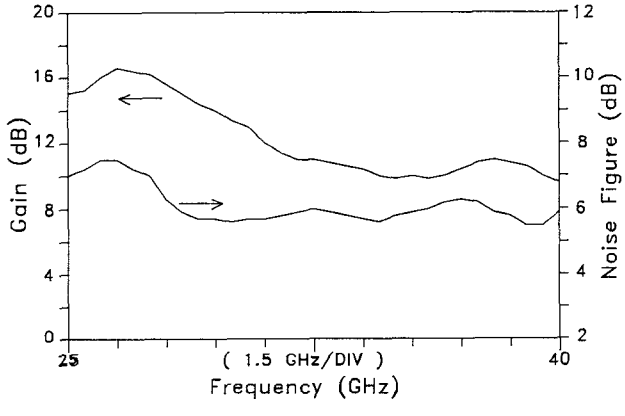


Figure 9. Measured performance for a two stage monolithic amplifier using two 75 um MESFETs.

CONCLUSIONS

A monolithic broadband LNA using MESFET technology has been demonstrated at Ka-band. A single stage design with about 5 dB gain and an average noise figure of 4.5 dB has been demonstrated. A two stage design has produced more than 10 dB gain and an average noise figure of 6 dB has been demonstrated over the full Ka-band. Lower noise figure numbers are expected when such MMICs are processed using optimized low noise MESFET devices.

ACKNOWLEDGMENT

The authors wish to thank R. Balbuena, R. C. Hansen, and F. N. Nostratis for their technical assistance. They also wish to thank A. Lee for his assistance with the E-beam Lithography.

REFERENCE

(1) C. YUEN, et al., "A Monolithic Ka-Band HEMT Low-Noise Amplifier," IEEE MTT-Symposium Digest, 1988, pp.247-250.